Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUCTIONS:**

1. **N. CLEAR**
2. **Q1**
3. **N. Q1**
4. **D1**
5. **D2**
6. **N. Q2**
7. **Q2**
8. **VSS**
9. **CLOCK**
10. **Q3**
11. **N. Q3**
12. **D3**
13. **D4**
14. **N. Q4**
15. **Q4**
16. **VDD**

**.077”**

**80**

**.065”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential: VDD**

**Mask Ref:**

**80**

**APPROVED BY: DK DIE SIZE .065” X .077” DATE: 10/20/21**

**MFG: RCA THICKNESS .020” P/N: CD40175B**

**DG 10.1.2**

#### Rev B, 7/1